DI-188 Design Idea
TOPSwitch®-HX

20 W Low No-load Consumption Power Supply

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
Generic	TOP255PN	20 W	85 – 265 VAC	12 V	Flyback

Design Highlights

- Very low no-load consumption: <100 mW (85-230 VAC)
- High active-on average efficiency:
  - 84.7% at 115 VAC,
  - 85.5% at 230 VAC
  - Easily meets ENERGY STAR 2.0 and EU CoC V3
- High standby output power at 230 VAC:
  - 0.75 W at 1.0 W input power
  - 0.35 W at 0.5 W input power
  - 0.2 W at 0.3 W input power
- Line sensing
  - Line feed-forward for excellent line ripple rejection
  - Intelligent brown-out protection
  - Undervoltage lockout (UVLO) with auto-restart
  - Extended line surge immunity (overvoltage shutdown (OV))
- No heat sink necessary
- Hysteretic thermal, overload and output short-circuit protection

Operation

The power supply design in Figure 1 features a TOPSwitch-HX TOP255PN in a flyback configuration, with universal input, and 12 V, 20 W output. This design offers energy-efficient performance with very low no-load input power consumption.

The TOP255PN (U1) converts a feedback current at the control input to a duty cycle at the open drain output of its integrated high-power MOSFET. IC U1 provides high-voltage start-up, cycle-by-cycle current limiting, loop compensation, auto-restart, thermal shutdown, a high-voltage (700 V) integrated MOSFET and control circuitry. The M pin provides a single input for overvoltage (OV), undervoltage (UV) and line feed-forward with DC_{MAX} reduction.

Fuse F1 provides catastrophic fault protection, isolating the circuit from the AC source. X-capacitor C1 reduces differential-mode EMI and is small enough to avoid the need for safety bleed resistors, per UL standard 60950-1. Y-capacitor C7 and common-mode inductor L1 filter common-mode EMI. Diodes D1 through D4 rectify the AC input; C2 filters the resulting DC. Capacitor C6 acts as a decoupling capacitor and C5 both sets the auto-restart timing and, with R6, provides control-loop compensation for U1.

The clamp network (VR1, R9, C3, R8, and D5) protects U1 from voltage spikes from leakage inductance on the transformer primary side at turn-off. Resistors R3 and R4 sense the DC bus voltage for line feed-forward information, UVLO startup voltage threshold value, and extended line surge immunity via OV

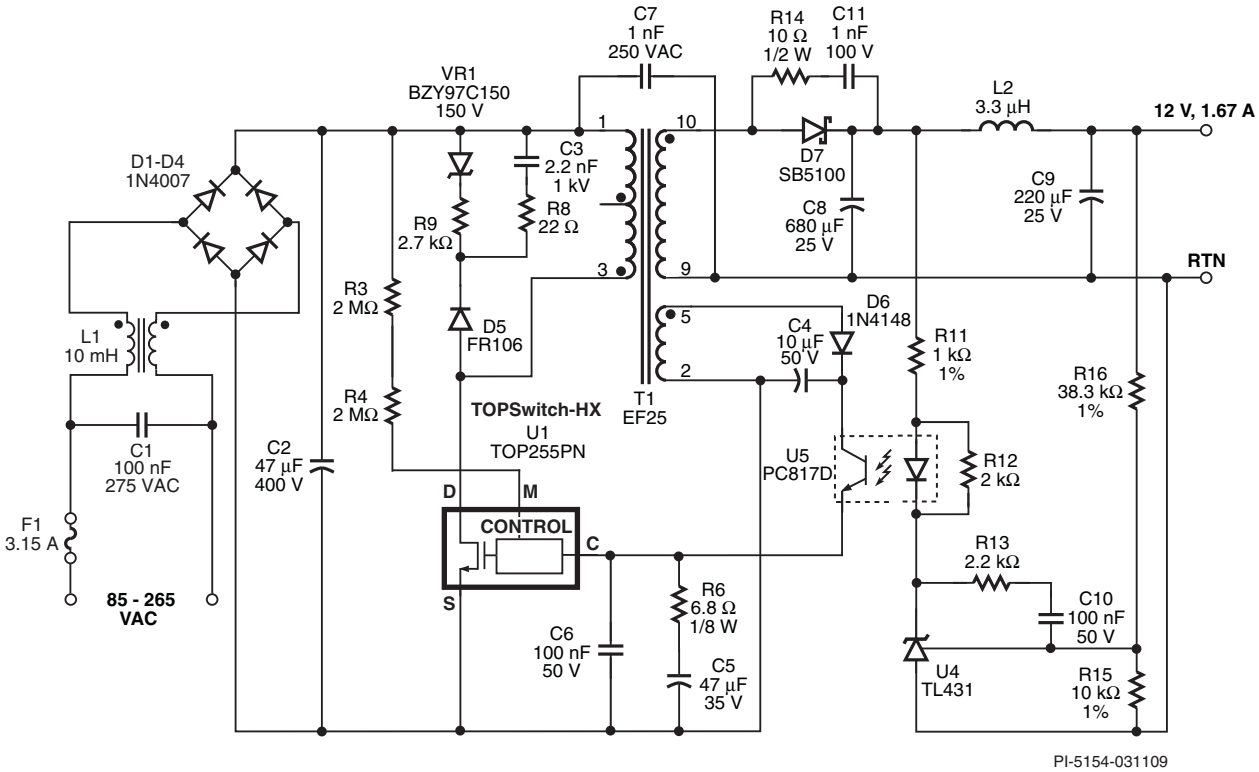

Figure 1. Schematic of a 20 W Power Supply with Very Low No-load Consumption Using TOP255PN .

shutdown. Zener diode VR1 does not conduct under no-load conditions, for reduced dissipation.

At high load the controller operates at full switching frequency (66 kHz). The internal current limit provides cycle-by-cycle current limit protection. A second current-limit comparator monitors the actual peak drain current (I_P) relative to the programmed current limit $I_{LIMITEXT}$. As soon as $I_P/I_{LIMITEXT}$ falls below 55%, the peak drain current stays constant and output is regulated through switching frequency modulation. The switching frequency reduces with load reduction linearly, down to 30 kHz. The 30 kHz is maintained, with the peak current controlled for output regulation until $I_P/I_{LIMITEXT}$ falls below 25%. Then the controller enters multi-cycle-modulation mode.

Diode D6 rectifies the bias output; C4 filters it, peak-charging caused by bias winding leakage spikes, keeps this voltage >10 V even under light or no-load conditions. Optocoupler U5 provides current directly to the C pin at a level to keep auto-restart enabled. This ensures that the optocoupler is biased and the control loop can maintain regulation.

Regulator IC U4 (400 μA typical minimum cathode current) needs no bias resistor and reduces no-load power. Resistors R15 and R16 sense the output voltage; R13 and C10 set the feedback circuit frequency response. Resistor R11 sets the overall DC loop gain and limits transient current through the diode in U5.

The snubber circuit (R14 and C11) is placed across secondary rectifier D7 and attenuates high-frequency ringing; inductor L2 and capacitor C9 form an output second-stage filter.

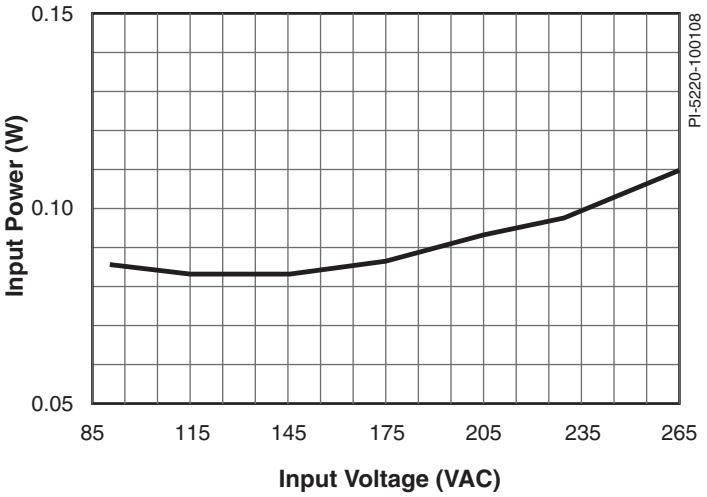

Figure 2. No Load Input Power vs Line Voltage.

Key Design Points

- Using a fast (rather than ultra-fast) recovery diode for D5 allows some clamp energy to be recovered for improved efficiency at light loads and reduced no-load consumption.
- High-gain optocoupler for U5, with a CTR of 300% to 600%, reduces secondary-side dissipation. Resistor R11 reduces no-load input power (by 30 mW) at 265 VAC.
- Small values for snubber components R14 and C11 reduce high-frequency ringing and no-load input power dissipation.

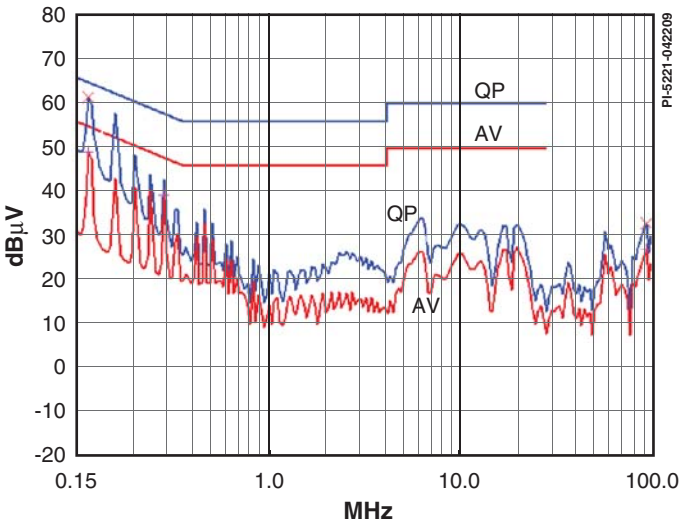

Figure 3. Conducted EMI Scan to EN55022 B Limits. Measurements Made at 230 VAC With Output RTN Connected to Artificial Hand, Representing Worst-case Conditions.

Transformer Parameters	
Core Material	EF25, gapped for ALG of 244 nH/t²
Bobbin	EF25, 5 primary + 5 secondary
Winding Details	Primary 1: 40T, 1 × 0.32 mm Feedback/Bias: 10T, 1 × 0.45 mm Secondary: 10T, 2 × 0.40 mm TIW Primary 2: 40T, 1 × 0.32 mm
Winding Order	First Half Primary (3–4), Feedback/Bias (5–2), Secondary (10–9), Second Half Primary (4–1)
Primary Inductance	1.56 mH, ±5%
Primary Resonant Frequency	1500 kHz (minimum)
Leakage Inductance	14 μH (maximum)

Table 1. Transformer Parameters. (TIW = Triple Insulated Wire)

Power Integrations
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1 408-414-9200
Customer Service
Phone: +1-408-414-9665
Fax: +1-408-414-9765
Email: usasales@powerint.com

On the Web
www.powerint.com