Design Example Report

Title	***High Efficiency 30 W Standby Power Supply Using TOPSwitch^{TM}-JX TOP265KG***
Specification	110 VDC – 400 VDC Input; 12 V, 2.5 A, Output
Application	Standby Supply
Author	Applications Engineering Department
Document Number	DER-275
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Revision	1.5

Summary and Features

- Highly energy efficient
  - Full load efficiency >89%
  - Efficiency >86% above 10% load
  - Average efficiency >89% (25%, 50%, 75%, 100% load points)
  - No-load input power <100 mW for input voltages <385 VDC
  - Simplifies meeting ENERGY STAR 2.0, 80 Plus and EuP requirements
- Low cost, low component count and small PCB footprint solution
  - Performance met without synchronous output rectification
  - 132 kHz operation optimized core size and efficiency performance
  - Surface mount low-profile eSOP package
- Integrated protection and reliability features
  - Line undervoltage lock out (UVLO)
  - Primary sensed output overvoltage shutdown (OVP). Latched OVP condition can be reset with a fast AC reset circuit.
  - Auto recovery output over current (OCP)
  - Meets limited power source (LPS) <100 VA requirement with a single point of failure
  - Accurate thermal shutdown with large hysteresis

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolated power source to provide the DC input to the prototype board.

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1 Introduction

This document is an engineering report describing standby power supply utilizing a TOPSwitch-JX TOP265KG. This power supply is intended as a general purpose evaluation platform that operates from 110 VDC to 400 VDC input and provides a 12 V, continuous 30 W output.

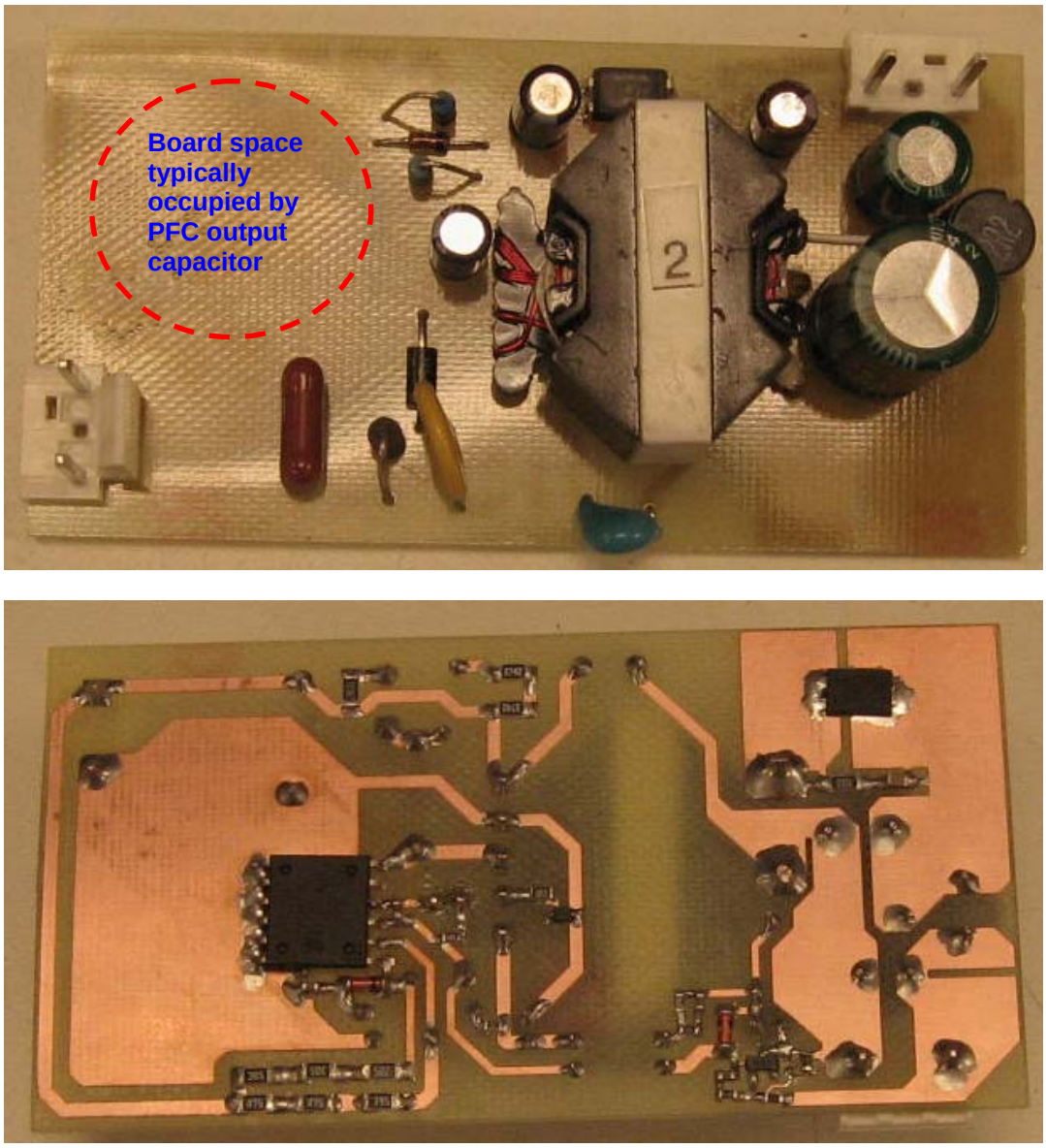

Figure 1 – Populated Circuit Board Photographs.

Note: This design eliminates need for external heat sink for the integrated power supply controller IC by making use of board space underneath the PFC output capacitor.

This standby supply was designed to meet 80 Plus Standard and Energy Star 2.0 >87% average-efficiency, no-load <100 mW for input voltage of 385 VDC or lower.

This power supply offers these various protection features using a low component count circuit:

- Overvoltage protection (OVP) with latching shutdown and optional fast AC reset
- Primary-side sensed output overload protection, even with a single fault
- Open-loop protection
- Auto-restart overload protection
- Accurate thermal overload protection with auto-recovery using a large hysteresis

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	110		400	VDC	
No-load Input Power (385 VDC)				0.1	W	
Output						
Output Voltage	V_{OUT}		12		V	± 5%
Output Ripple Voltage	V_{RIPPLE}			120	mV	20 MHz bandwidth
Output Current	I_{OUT}	0		2.5	A	
Total Output Power						
Continuous Output Power	P_{OUT}	30			W	
Efficiency						
Full Load	η	88			%	Measured at P_{OUT} 25 °C
Required average efficiency at 25, 50, 75 and 100 % of P_{OUT}	$\eta_{ES2.0}$	83			%	Per ENERGY STAR V2.0
Protection						
Over Power				60	W	Auto-recovery
Overvoltage				25	VDC	Latching
Environmental						
Safety		Designed to meet IEC950 / UL1950 Class II				
Ambient Temperature	T_{AMB}	0	25	40	°C	Free convection, sea level

3 Schematic

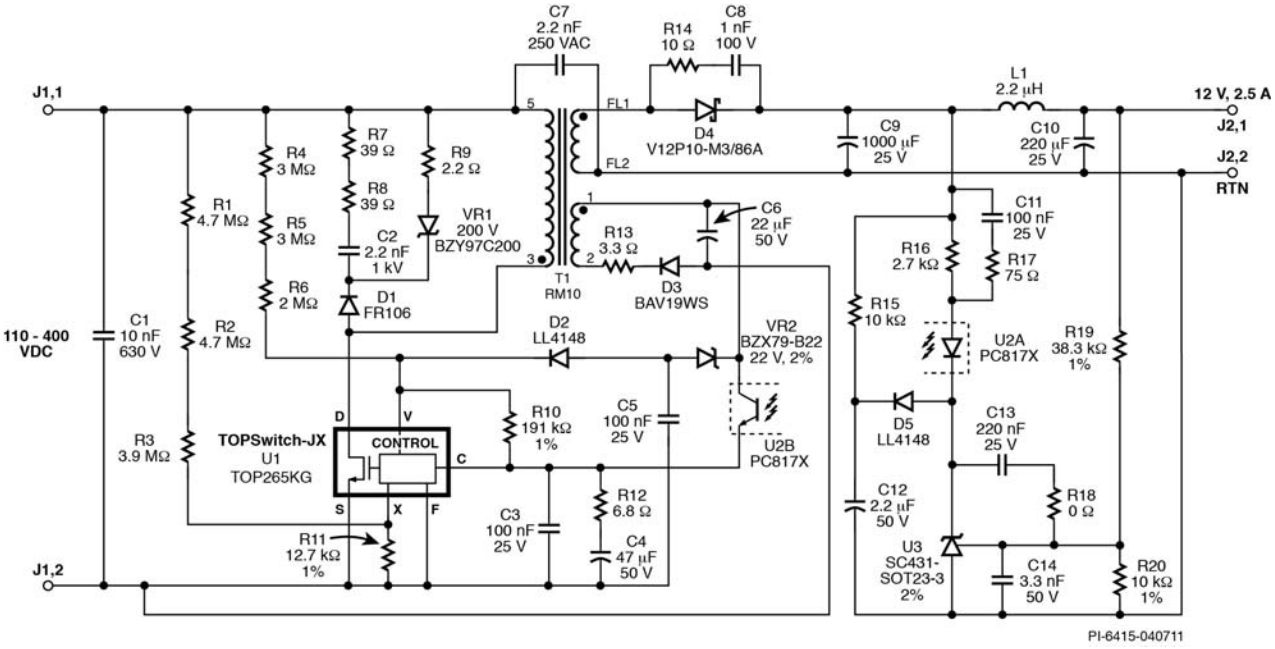

Figure 2 – Schematic.

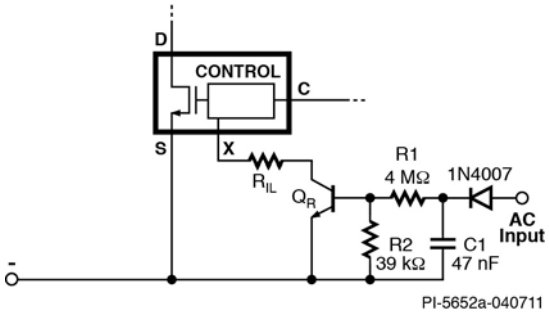

Figure 3 – Fast AC Reset Circuit.

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4 Circuit Description

This flyback converter configuration, built around the TOP265KG (U1), provides a 12 V output, and delivers a load current of 2.5 A. This power supply operates over an input range of 110 VDC to 400 VDC. The output is secondary-side regulated using voltage reference U3.

4.1 TOPSwitch-JX Primary

Resistors R4, R5 and R6 provide a current into the VOLTAGE MONITOR (V) pin of U1 proportional to the DC voltage across high-voltage bypass capacitor C1. Resistor R10 provides an offset current into the V pin to reduce the current drawn from the DC bus via R4, R5 and R6. This reduces the dissipation in R4, R5 and R6 which significantly reduces no-load and light load input power. The values shown set the under voltage threshold to 80 VDC, the point at which current into the V pin exceeds 25 μA. At this point switching is enabled and the power supply starts up.

An RCDZ clamp network (D1, R7, R8, R9, C2 and VR1) limits the drain voltage of U1 to below 725 V after the MOSFET inside U1 turns OFF. This configuration was selected as it maximizes efficiency across the load range.

Diode D3 rectifies the bias winding output of transformer T1. Resistor R13 and capacitor C6 filter the output of the bias winding. This provides the necessary bias supply for the optocoupler U2B. The voltage across capacitor C6 was adjusted via the bias winding turns to be ~9 V at no-load and 400 VDC input. This voltage value minimizes no-load consumption but ensures that sufficient voltage is present on the optocoupler collector to maintain regulation.

The secondary-side feedback circuitry maintains output voltage regulation via U2A. A change in current through the optocoupler diode causes a change in the current out of the optocoupler transistor (which is proportional to the CTR of the optocoupler) and into CONTROL (C) pin of IC U1. Current into the C pin changes the duty cycle of the internal MOSFET thereby regulating the output voltage.

Zener diode VR2 provides output overvoltage protection. Any fault condition which causes the power supply output to exceed regulation limits also causes the voltage across the bias winding to increase. Consequently, Zener diode VR2 breaks down and sufficient current flows into the V pin of U1 via D2 to initiate OVP. A resistor can be added in series with VR2 that limits the current into the V pin and changes the latching to self recovering shutdown.

Resistors R1, R2, R3 and R11 provide output power limiting. By reducing the current limit as a function of the input voltage a relatively constant overload power is achieved.

4.2 Output Rectification

Diode D4 provides rectification for the 12 V output, and low-ESR capacitor C9 provides filtering. To eliminate high frequency switching noise, a post filter was added (L1 and C10).

The snubber network comprised of R14 and C8 damp oscillations on D4 caused by the transformer winding leakage inductance, reducing radiated EMI and diode voltage stress.

4.3 Output Feedback

The output voltage is controlled using shunt regulator U3. Resistors R19 and R20 sense the output voltage, forming a resistor divider connected to the reference input of IC U3. Changes in the output voltage and hence the voltage at the reference input of U3 results in changes in the cathode voltage of IC U3 and therefore optocoupler LED current. This changes the current into the C pin of U1 and acts to maintain output regulation.

Capacitor C13 introduces a pole at DC, rolling off the gain of U3. Resistor R17 and capacitor C11 provides the additional phase boost to achieve stable power supply operation. Capacitor C14 was added after it was found that switching noise was being injected into the reference pin of IC U3.

Resistor R16 sets the overall loop gain and limits current through U3A during transient conditions.

To reduce power dissipation in the feedback circuit (and lower no-load consumption) a D rank optocoupler was selected with the value of resistor R16 increased to offset the increase in loop gain. A low minimum cathode current (150 μA) reference was selected for U3 to also reduce dissipation.

4.4 Fast AC Reset

The TOPSwitch-JX family has a fast AC reset function which can be configured on the EXTERNAL CURRENT LIMIT (X) pin (as shown in Figure 3). Should the device stop switching due to a latching OVP fault condition, the circuit connected to the X pin will force I_X to exceed $I_{X(TH)}$ = -27 μA (typical) and reset the latch when the AC input is disconnected or falls below a set threshold value.

In Figure 3, R1, R2 and C1 set the time after AC is removed before the latch is reset. A higher gain BJT Q_R is desirable to allow a higher resistance value for R1 and lower capacitance value for C1, and thus minimize the circuit dissipation.

Consult Application Note AN-47 TOPSwitch-JX Family Design Guide for further information.

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5 PCB Layout

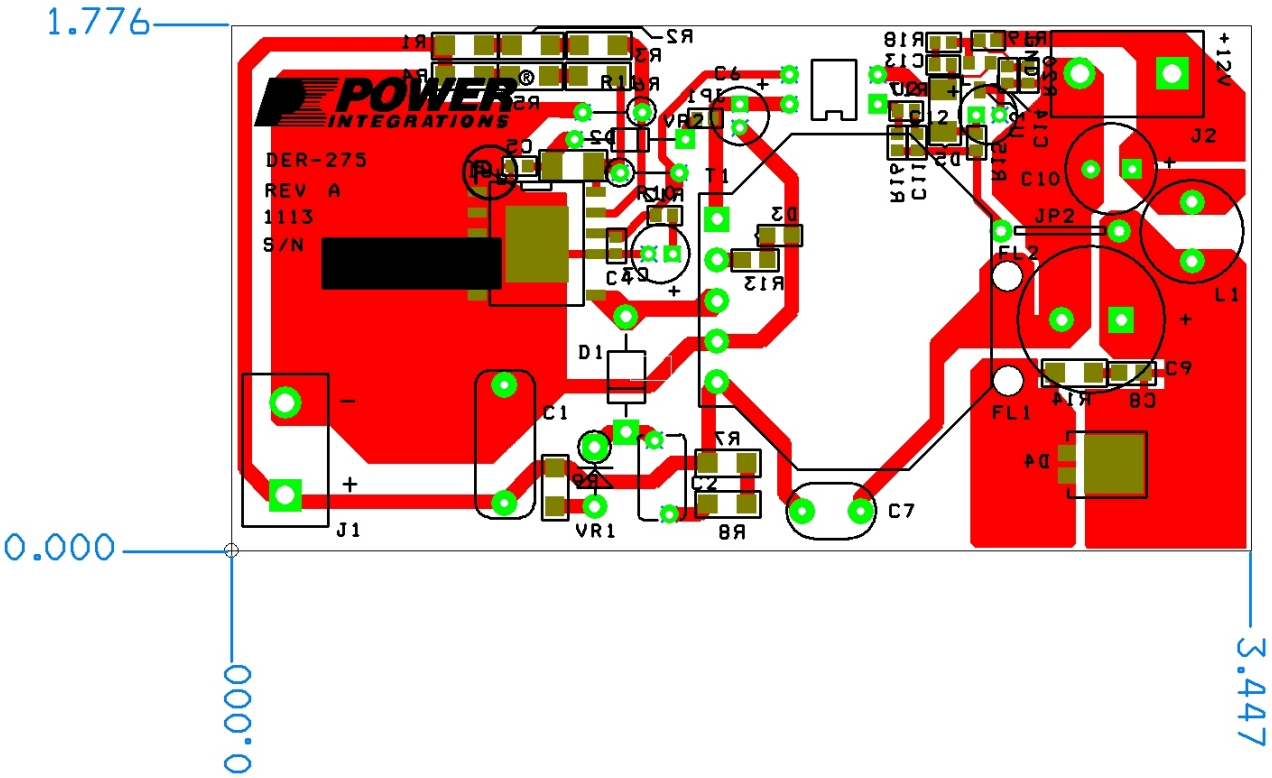

Figure 4 – Printed Circuit Layout (1.776” x 3.447”)

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	C1	10 nF, 630 V, Film	ECQ-E6103KF	Panasonic
2	1	C2	2200 pF, 1 kV, Disc Ceramic	562R5GAD22	Vishay
3	3	C3 C5 C11	100 nF 25 V, Ceramic, X7R, 0603	ECJ-1VB1E104K	Panasonic
4	1	C4	47 µF, 25 V, Electrolytic, Gen. Purpose, (5 x 11)	ECA-1EM470	Panasonic
5	1	C6	22 µF, 50 V, Electrolytic, Low ESR, 900 mΩ, (5 x 11.5)	ELXZ500ELL220MEB5D	Nippon Chemi-Con
6	1	C7	2.2 nF, 250 VAC, Film, X1Y1	DE2E3KY222MA2BM01	Murata
7	1	C8	1 nF, 100 V, Ceramic, X7R, 0805	ECJ-2VB2A102K	Panasonic
8	1	C9	1000 µF, 25 V, Electrolytic, Very Low ESR, 21 mΩ, (12.5 x 20)	EKZE250ELL102MK20S	Nippon Chemi-Con
9	1	C10	220 µF, 25 V, Electrolytic, Very Low ESR, 72 mΩ, (8 x 11.5)	EKZE250ELL221MHB5D	Nippon Chemi-Con
0	1	C12	2.2 µF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKME500ELL2R2ME11D	Nippon Chemi-Con
11	1	C13	220 nF, 25 V, Ceramic, X7R, 0603	06033D224KAT2A	AVX
12	1	C14	3.3 nF, 50 V, Ceramic, X7R, 0603	GRM188R71H332KA01D	Murata
13	1	D1	800 V, 1 A, Fast Recovery Diode, 500 ns, DO-41	FR106	Diodes, Inc.
14	2	D2 D5	75 V, 0.15 A, Fast Switching, 4 ns, MELF	LL4148-13	Diodes, Inc.
15	1	D3	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
16	1	D4	100 V, 12 A, Schottky, SMD, TO-277A	V12P10-M3/86A	Vishay/General Semi
17	2	FL1 FL2	PCB Terminal Hole, #22 AWG	N/A	N/A
18	2	J1 J2	2 Position (1 x 2) header, 0.312 pitch, Vertical	26-50-3039	Molex
19	1	JP1	0 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic
20	1	L1	2.2 µH, 6.0 A	RFB0807-2R2L	Coilcraft
21	2	R1 R2	4.7 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ475V	Panasonic
22	1	R3	3.9 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ395V	Panasonic
23	2	R4 R5	3 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ305V	Panasonic
24	1	R6	2 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ205V	Panasonic
25	2	R7 R8	39 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ390V	Panasonic
26	1	R9	2.2 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ2R2V	Panasonic
27	1	R10	191 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-191K	Yageo
28	1	R11	12.7 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-12K7	Yageo
29	1	R12	6.8 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ685V	Panasonic
30	1	R13	3.3 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ3R3V	Panasonic
31	1	R14	10 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ100V	Panasonic
32	1	R15	10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
33	1	R16	2.7 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ272V	Panasonic
34	1	R17	75 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ750V	Panasonic
35	1	R18	0 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic

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36	1	R19	38.3 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3832V	Panasonic
37	1	R20	10 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1002V	Panasonic
38	1	T1	Bobbin, RM10, Vertical, 5 pins	P-1031	Pin Shine
39	1	U1	TOPSwitch-JX, eSOP-12	TOP265KG	Power Integrations
40	1	U2	Optocoupler, 35 V, CTR 300-600%, 4-DIP	PC817X4J000F	Sharp
41	1	U3	Shunt Regulator 2.5-30 V, 2%, SOT23-3	SC431CSK-2TRT	Semtech
42	1	VR1	200 V, 1.5 W, DO-41	BZY97C200-TR	Vishay
43	1	VR2	22 V, 500 mW, 2%, DO-35	BZX79-B22	Taiwan Semi

7 Transformer Specification

7.1 Electrical Diagram

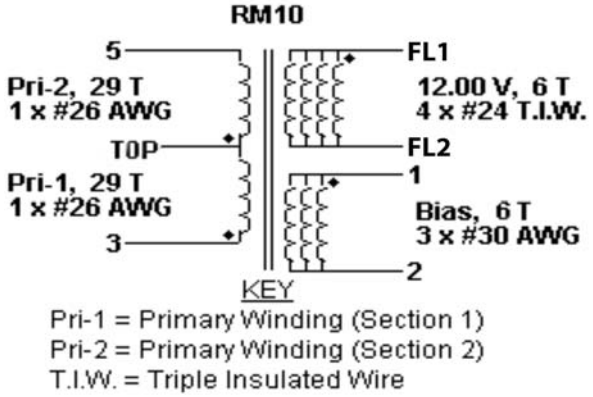

Figure 5 –Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	60 Hz 1 second, from pins 1, 2, 3, 4, 5 to pins FL1, FL2.	3000 VAC
Primary Inductance	Measured at 1 V pk-pk, typical switching frequency, between pin 3 to pin 5, with all other windings open.	2263 µH ±7%
Primary Leakage Inductance	Measured between pin 3 to pin 5, with all other windings shorted.	25 µH

7.3 Materials

Item	Description
[1]	Core: RM10, 3F3 or Equivalent, gapped for ALG of 682 nH/t²
[2]	Bobbin: Generic, 5 primary + 0 secondary
[3]	Barrier Tape: Polyester film (1 mil base thickness), 9.60 mm wide
[4]	Separation Tape: Polyester film (1 mil base thickness), 9.60 mm wide
[5]	Varnish
[6]	Magnet Wire: #26 AWG, Solderable Double Coated
[7]	Magnet Wire: #30 AWG, Solderable Double Coated
[8]	Triple Insulated Wire: #24 AWG

7.4 Comments

1. Use of a grounded flux-band around the core may improve the EMI performance.
2. For non margin wound transformers use triple insulated wire for all secondary windings.

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7.5 Transformer Build Diagram

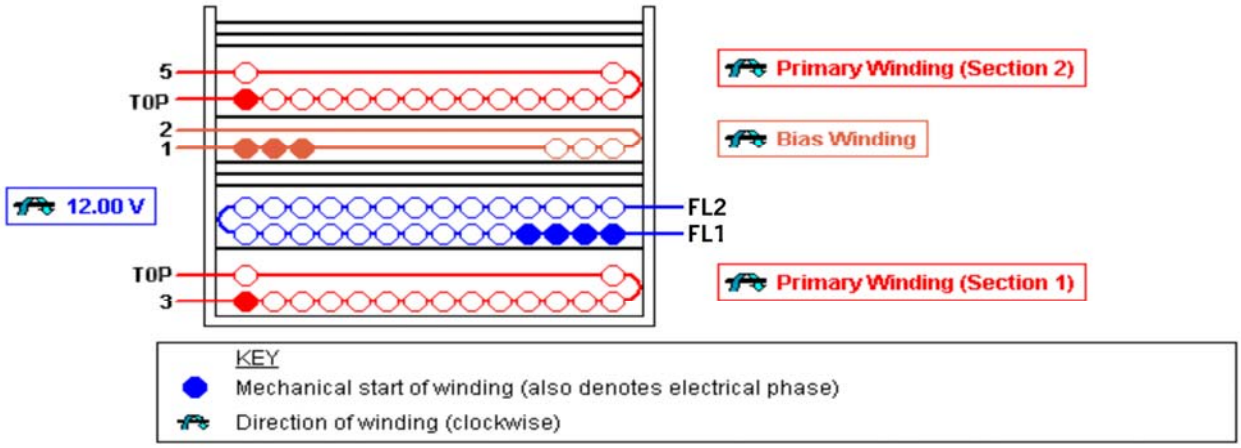

Figure 6 – Transformer Build Diagram.

7.6 Winding Instructions

Primary Winding (Section 1)	Start on pin(s) 3 and wind 29 turns (x 1 filar) of item [6] in 2 layer(s) from left to right. At the end of 1st layer, continue to wind the next layer from right to left. On the final layer, spread the winding evenly across entire bobbin. Finish this winding on pin(s) TOP. Add 1 layer of tape, item [3], for insulation.
Secondary Winding	Start on pin(s) FL1* and wind 6 turns (x 4 filar) of item [7]. Spread the winding evenly across entire bobbin. Wind in same rotational direction as primary winding. Finish this winding on pin(s) FL2*. Add 3 layers of tape, item [3], for insulation.
Bias Winding	Start on pin(s) 1 and wind 6 turns (x 3 filar) of item [8]. Wind in same rotational direction as primary winding. Spread the winding evenly across entire bobbin. Finish this winding on pin(s) 2. Add 3 layers of tape, item [3], for insulation.
Primary Winding (Section 2)	Start on pin(s) TOP and wind 29 turns (x 1 filar) of item [6] in 2 layer(s) from left to right. At the end of 1st layer, continue to wind the next layer from right to left. On the final layer, spread the winding evenly across entire bobbin. Finish this winding on pin(s) 5. Add 3 layers of tape, item [3], for insulation.
Core Assembly	Assemble and secure core halves. Item [1].
Varnish	Dip varnish uniformly in item [5]. Do not vacuum impregnate.

*Flying Lead. Flying leads were required for this design to meet safety spacing requirements, the RM10 bobbin spacing from core to secondary pins is less than the required >6mm.

8 Transformer Design Spreadsheet

ACDC TOPSwitch-JX 081810; Rev.1.4; Copyright Power Integrations 2010	INPUT	INFO	OUTPUT	UNIT	TOP_JX_081810: TOPSwitch-JX Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	12.00			Volts	Output Voltage (main)
PO_AVG	30.00			Watts	Average Output Power
PO_PEAK			30.00	Watts	Peak Output Power
Heatsink Type	**PCB**		PCB		Heatsink Type
Enclosure	**Open Frame**				Open Frame enclosure assume sufficienct airflow while adapter means a sealed enclosure.
N	0.90			%/100	Efficiency Estimate
Z	0.50				Select 'H' for Half frequency - 66kHz, or 'F' for Full frequency - 132kHz
VB	12			Volts	Bias Voltage - Verify that VB is > 8 V at no load and VMAX
tC	3.00			ms	Bridge Rectifier Conduction Time Estimate
CIN	220.0		220	uFarads	Input Filter Capacitor
ENTER TOPSWITCH-JX VARIABLES					
TOPSwitch-JX	**TOP265K**			Universal / Peak	115 Doubled/230V
Chosen Device		*TOP265K*	Power Out	34 W / 34 W	53W
KI	0.48				External Ilimit reduction factor (KI=1.0 for default ILIMIT, KI <1.0 for lower ILIMIT)
ILIMITMIN_EXT			0.759	Amps	Use 1% resistor in setting external ILIMIT
ILIMITMAX_EXT			0.873	Amps	Use 1% resistor in setting external ILIMIT
Frequency (F)=132kHz, (H)=66kHz	**F**		F		Select 'H' for Half frequency - 66kHz, or 'F' for Full frequency - 132kHz
fS			132000	Hertz	TOPSwitch-JX Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin			119000	Hertz	TOPSwitch-JX Minimum Switching Frequency
fSmax			145000	Hertz	TOPSwitch-JX Maximum Switching Frequency
High Line Operating Mode			FF		Full Frequency, Jitter enabled
VOR	120.00			Volts	Reflected Output Voltage
VDS			10	Volts	TOPSwitch on-state Drain to Source Voltage
VD	0.50			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.70			Volts	Bias Winding Diode Forward Voltage Drop
KP	0.34	*Info*			A minimum KP of 0.4 is recommended for Low Line or Universal input supplies.
PROTECTION FEATURES					
LINE SENSING					V pin functionality
VUV_STARTUP			94	Volts	Minimum DC Bus Voltage at which the power supply will start-up
VOV_SHUTDOWN			445	Volts	Typical DC Bus Voltage at which power supply will shut-down (Max)
RLS			4.0	M-ohms	Use two standard, 2 M-Ohm, 5% resistors in series for line sense functionality.
OUTPUT OVERVOLTAGE					
VZ			22	Volts	Zener Diode rated voltage for Output Overvoltage shutdown protection
RZ			5.1	k-ohms	Output OVP resistor. For latching

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					shutdown use 20 ohm resistor instead
OVERLOAD POWER LIMITING					X pin functionality
Overload Current Ratio at VMAX			1.2		Enter the desired margin to current limit at VMAX. A value of 1.2 indicates that the current limit should be 20% higher than peak primary current at VMAX
Overload Current Ratio at VMIN			1.14		Margin to current limit at low line.
ILIMIT_EXT_VMIN			0.67	A	Peak primary Current at VMIN
ILIMIT_EXT_VMAX			0.44	A	Peak Primary Current at VMAX
RIL			12.72	k-ohms	Current limit/Power Limiting resistor.
RPL			N/A	M-ohms	Resistor not required. Use RIL resistor only
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**RM10**		RM10		Core Type
Core		*#N/A*		*P/N:*	#N/A
Bobbin		*#N/A*		*P/N:*	#N/A
AE	0.8900		0.89	cm^2	Core Effective Cross Sectional Area
LE	3.3900		3.39	cm	Core Effective Path Length
AL	5200.0		5200	nH/T^2	Ungapped Core Effective Inductance
BW	9.6		9.6	mm	Bobbin Physical Winding Width
M	0.00			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3.00				Number of Primary Layers
NS	6		6		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN	110		110	Volts	Minimum DC Input Voltage
VMAX	400		400	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.55		Maximum Duty Cycle (calculated at PO_PEAK)
IAVG			0.30	Amps	Average Primary Current (calculated at average output power)
IP			0.67	Amps	Peak Primary Current (calculated at Peak output power)
IR			0.23	Amps	Primary Ripple Current (calculated at average output power)
IRMS			0.41	Amps	Primary RMS Current (calculated at average output power)
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			2263	uHenries	Primary Inductance
LP Tolerance	7		7		Tolerance of Primary Inductance
NP			58		Primary Winding Number of Turns
NB			6		Bias Winding Number of Turns
ALG			682	nH/T^2	Gapped Core Effective Inductance
BM			2955	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP			4124	Gauss	Peak Flux Density (BP<4200) at ILIMITMAX and LP_MAX. Note: Recommended values for adapters and external power supplies <=3600 Gauss
BAC			502	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
Ur			1576		Relative Permeability of Ungapped Core
LG			0.14	mm	Gap Length (Lg > 0.1 mm)
BWE			28.8	mm	Effective Bobbin Width
OD			0.50	mm	Maximum Primary Wire Diameter including insulation
INS			0.07	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.43	mm	Bare conductor diameter
AWG			26	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			256	Cmils	Bare conductor effective area in circular mils

CMA		*Warning*	620	Cmils/Amp	!!! DECREASE CMA> (decrease L(primary layers),increase NS,smaller Core)
Primary Current Density (J)			3.22	Amps/mm^2	!!! Info. Primary current density is low. Can increase Primary current density. Reduce primary layers, or use smaller core
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			6.43	Amps	Peak Secondary Current
ISRMS			3.62	Amps	Secondary RMS Current
IO_PEAK			2.50	Amps	Secondary Peak Output Current
IO			2.50	Amps	Average Power Supply Output Current
IRIPPLE			2.62	Amps	Output Capacitor RMS Ripple Current
CMS			724	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			21	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.73	mm	Secondary Minimum Bare Conductor Diameter
ODS			1.60	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.44	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			636	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			54	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			54	Volts	Bias Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			12	Volts	Output Voltage
IO1_AVG			2.50	Amps	Average DC Output Current
PO1_AVG			30.00	Watts	Average Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			6.00		Output Winding Number of Turns
ISRMS1			3.621	Amps	Output Winding RMS Current
IRIPPLE1			2.62	Amps	Output Capacitor RMS Ripple Current
PIVS1			54	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS1			724	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			21	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.73	mm	Minimum Bare Conductor Diameter
ODS1			1.60	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2_AVG				Amps	Average DC Output Current
PO2_AVG			0.00	Watts	Average Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			0.34		Output Winding Number of Turns
ISRMS2			0.000	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire

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3rd output					
VO3				Volts	Output Voltage
IO3_AVG				Amps	Average DC Output Current
PO3_AVG			0.00	Watts	Average Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.34		Output Winding Number of Turns
ISRMS3			0.000	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			2	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total Continuous Output Power			30	Watts	Total Continuous Output Power
Negative Output			N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

Note: The warning about high CMA indicates that this may be an overdesign. This indicates that it may be possible to use thinner gauge wire.

9 Performance Data

All measurements performed at room temperature.

9.1 Full load Efficiency

Efficiency data points were recorded after 30 minutes soak time at 25 ºC ambient.

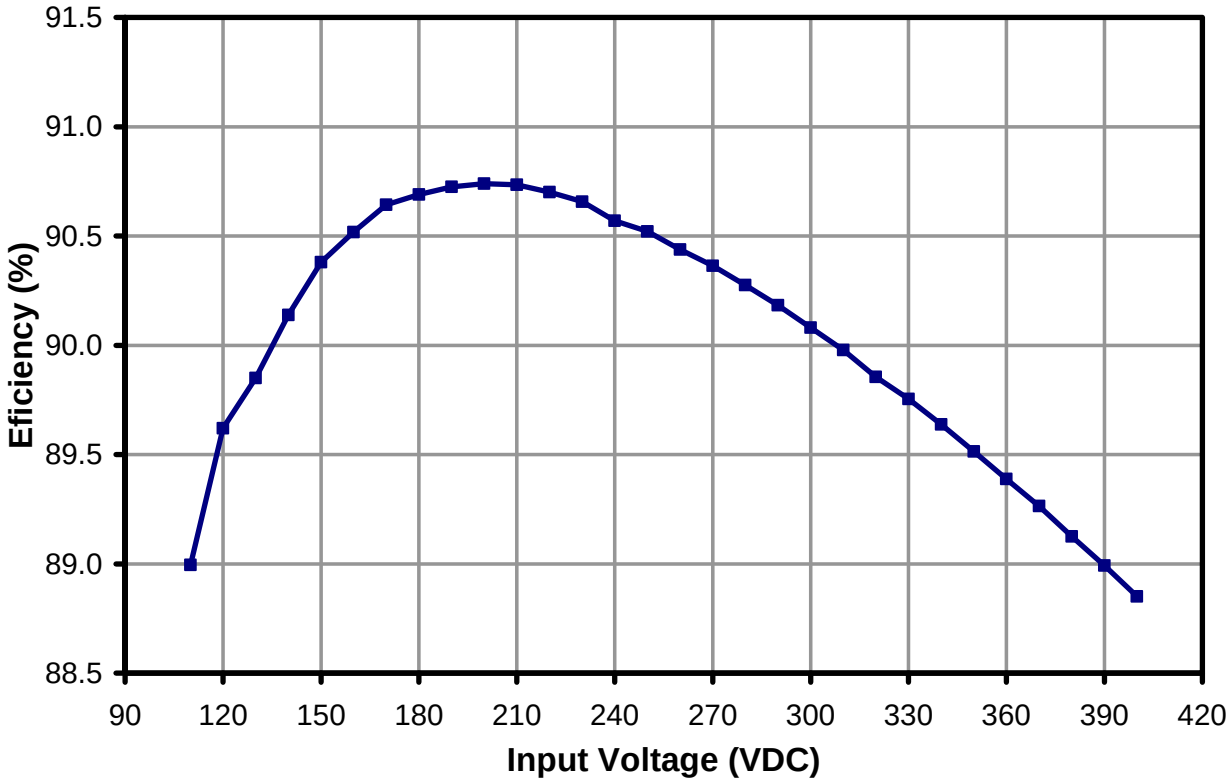

Figure 7 – Efficiency vs. Line Voltage, Full Load, Room Temperature.

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V_{IN} (V)	I_{IN} (A)	V_O (V)	I_O (A)	Efficiency
110	0.3076	12.045	2.5	88.99545
120	0.28	12.045	2.5	89.62054
130	0.2578	12.045	2.5	89.85051
140	0.2386	12.044	2.5	90.13891
150	0.2221	12.044	2.5	90.37971
160	0.2079	12.044	2.5	90.51828
170	0.1954	12.044	2.5	90.64363
180	0.18445	12.044	2.5	90.69004
190	0.17466	12.043	2.5	90.72514
200	0.1659	12.043	2.5	90.7399
210	0.15801	12.043	2.5	90.73416
220	0.15087	12.042	2.5	90.70121
230	0.14438	12.042	2.5	90.6575
240	0.13851	12.043	2.5	90.56957
250	0.13303	12.042	2.5	90.52094
260	0.12802	12.041	2.5	90.43809
270	0.12339	12.042	2.5	90.36389
280	0.1191	12.042	2.5	90.27528
290	0.11511	12.042	2.5	90.1836
300	0.1114	12.042	2.5	90.08079
310	0.10793	12.042	2.5	89.97767
320	0.1047	12.042	2.5	89.85494
330	0.10164	12.042	2.5	89.75529
340	0.09878	12.042	2.5	89.6377
350	0.09609	12.042	2.5	89.51429
360	0.09356	12.043	2.5	89.38857
370	0.09115	12.042	2.5	89.2648
380	0.08889	12.042	2.5	89.12553
390	0.08674	12.042	2.5	88.99275
400	0.08472	12.044	2.5	88.85151

Table 1 – Efficiency Data with Line Voltage Variation at Full Load.

9.2 Active Mode Efficiency

Data must be gathered at the following load points 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 15, 20, 25, 30, 40, 50, 60, 70, 75, 80, 90 and 100 % load with 380 VDC input voltage

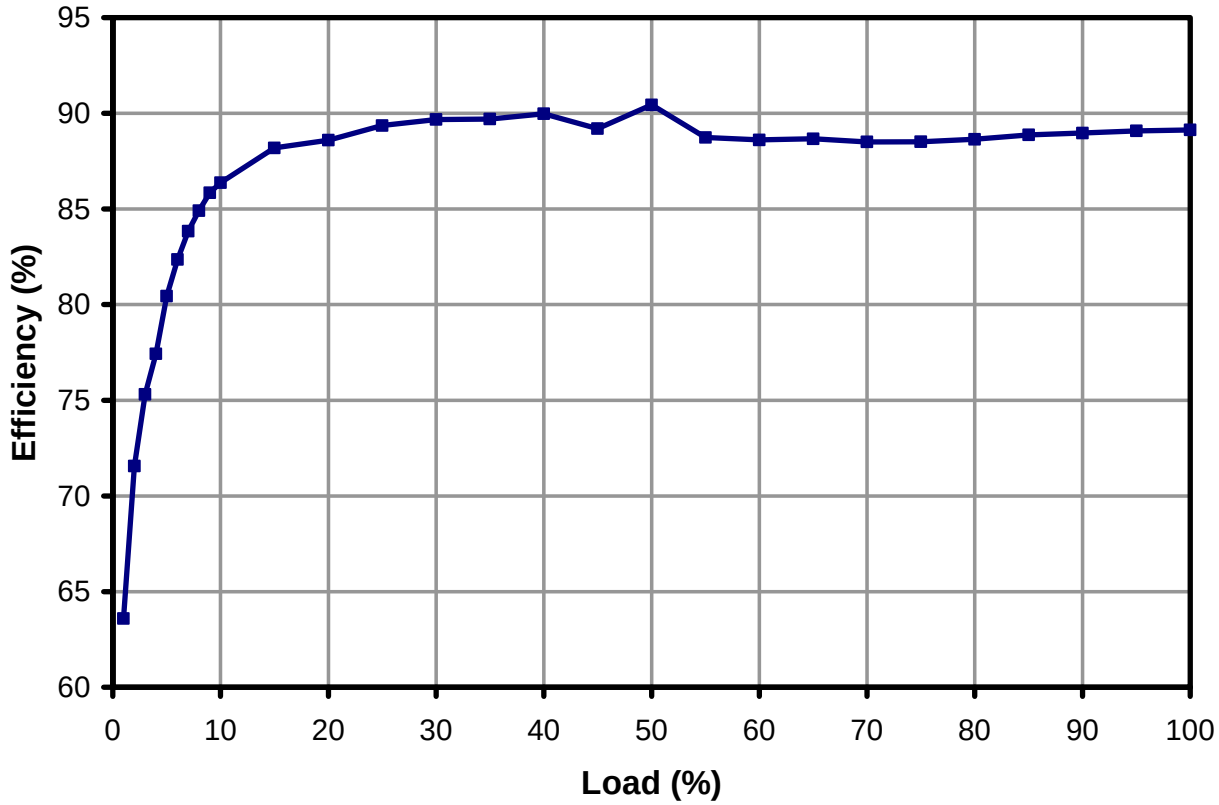

Figure 8 – Efficiency vs. Load Current (1-100%), Room Temperature.

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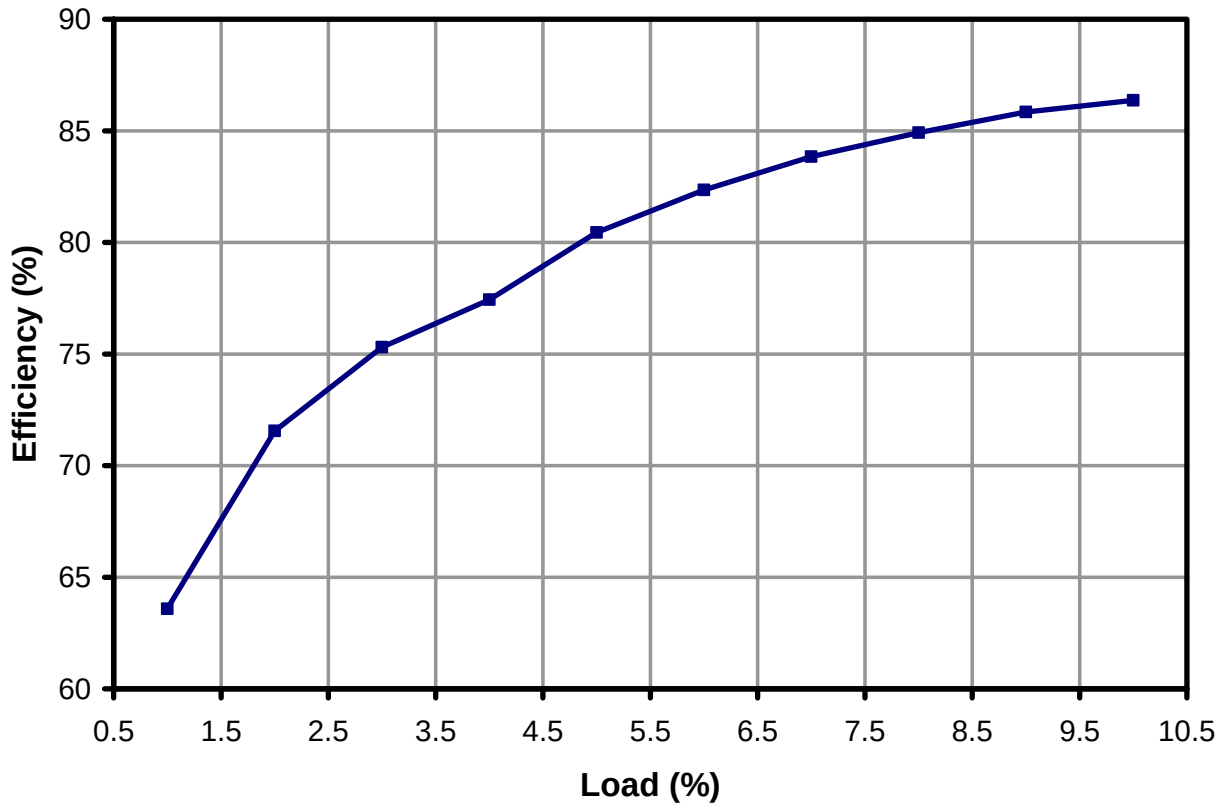

Figure 9 – Efficiency vs. Load Current (1-10%), Room Temperature.

V_{IN} (V)	I_{IN} (A)	V_O (V)	I_O (A)	Efficiency (%)	Load (%)
380	0.0889	12.044	2.5	89.13031	100
380	0.08449	12.043	2.375	89.08599	95
380	0.08015	12.043	2.25	88.96723	90
380	0.07577	12.043	2.125	88.88178	85
380	0.07151	12.044	2	88.64421	80
380	0.06714	12.044	1.875	88.51301	75
380	0.06267	12.044	1.75	88.50453	70
380	0.05809	12.044	1.625	88.66233	65
380	0.05365	12.044	1.5	88.61529	60
380	0.04911	12.044	1.375	88.7401	55
380	0.0438	12.043	1.25	90.44551	50
380	0.03997	12.043	1.125	89.20095	45
380	0.03522	12.042	1	89.97579	40
380	0.03091	12.041	0.875	89.69908	35
380	0.0265	12.041	0.75	89.67974	30
380	0.02216	12.041	0.625	89.36948	25
380	0.01788	12.04	0.5	88.60238	20
380	0.013472	12.039	0.375	88.18729	15
380	0.009169	12.037	0.25	86.36797	10
380	0.008302	12.037	0.225	85.84884	9
380	0.00746	12.036	0.2	84.91604	8
380	0.006611	12.036	0.175	83.84351	7
380	0.005769	12.036	0.15	82.35487	6
380	0.004921	12.035	0.125	80.44872	5
380	0.00409	12.035	0.1	77.43534	4
380	0.003154	12.035	0.075	75.31163	3
380	0.002213	12.035	0.05	71.55683	2
380	0.001245	12.034	0.025	63.59121	1

Table 2 – Efficiency Data with Load Variation at 380 VDC Input.

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9.3 No-load Input Power

DC Input supply without EMI filter.

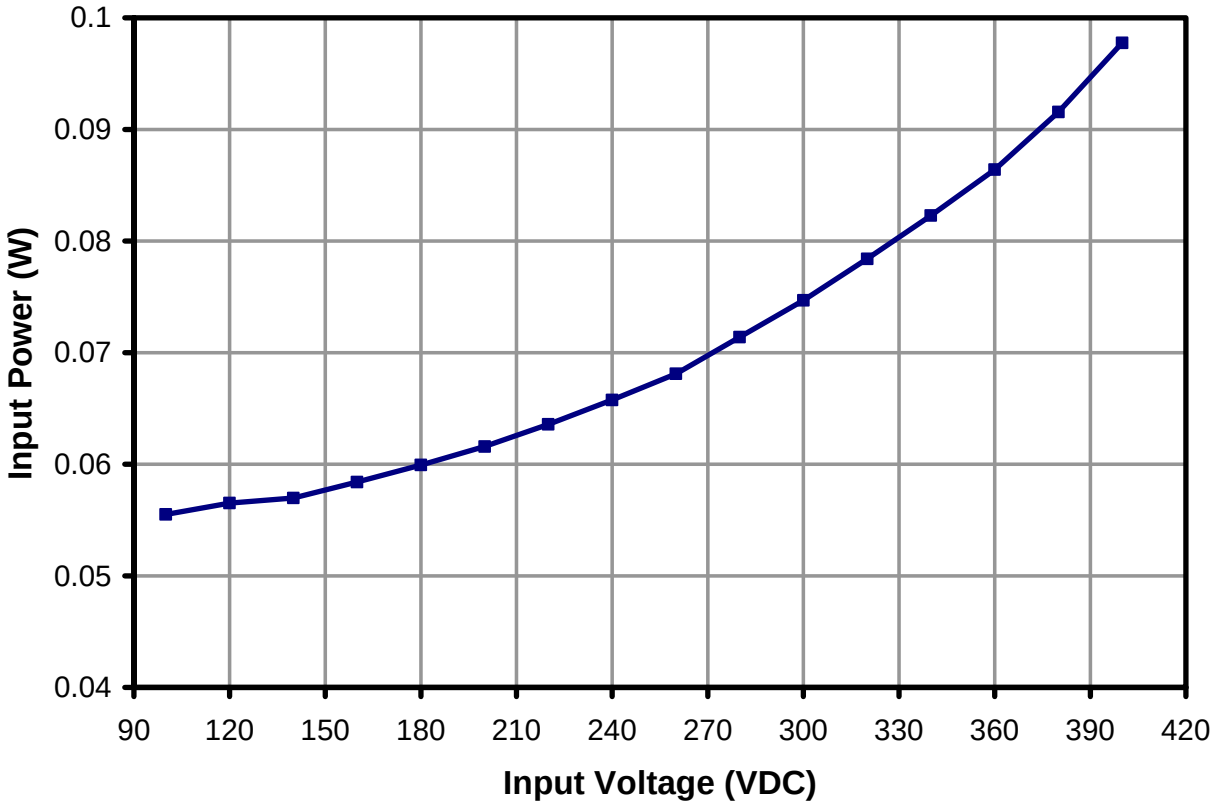

Figure 10 – Zero Load Input Power vs. Input Line Voltage, Room Temperature.

V_{IN} (VDC)	I_{IN} (A)	P_{IN} (W)
100	0.000555	0.0555
120	0.000471	0.05652
140	0.000407	0.05698
160	0.000365	0.0584
180	0.000333	0.05994
200	0.000308	0.0616
220	0.000289	0.06358
240	0.000274	0.06576
260	0.000262	0.06812
280	0.000255	0.0714
300	0.000249	0.0747
320	0.000245	0.0784
340	0.000242	0.08228
360	0.00024	0.0864
380	0.000241	0.09158
400	0.0002444	0.09776

Table 3 – No-Load Power.

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9.4 Regulation

9.4.1 Load Regulation

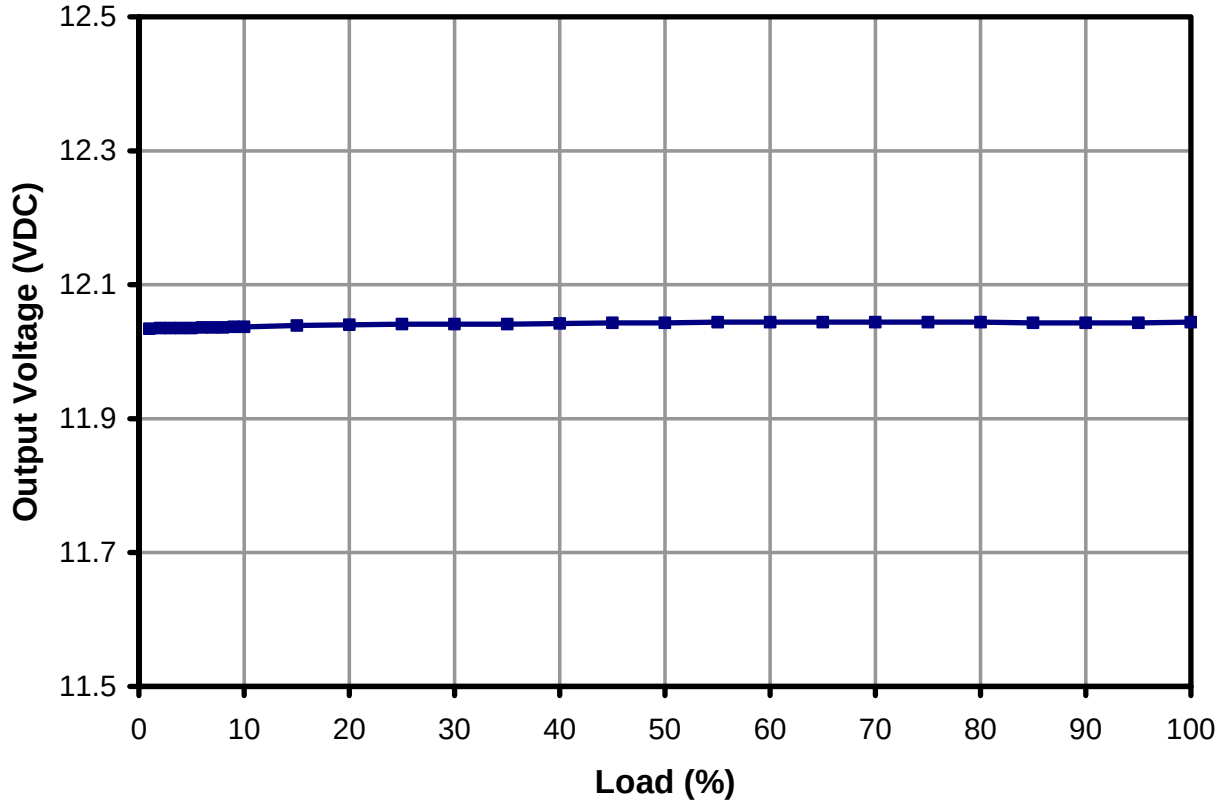

Figure 11 – Load Regulation, Room Temperature, 380 VDC.

9.4.2 Line Regulation

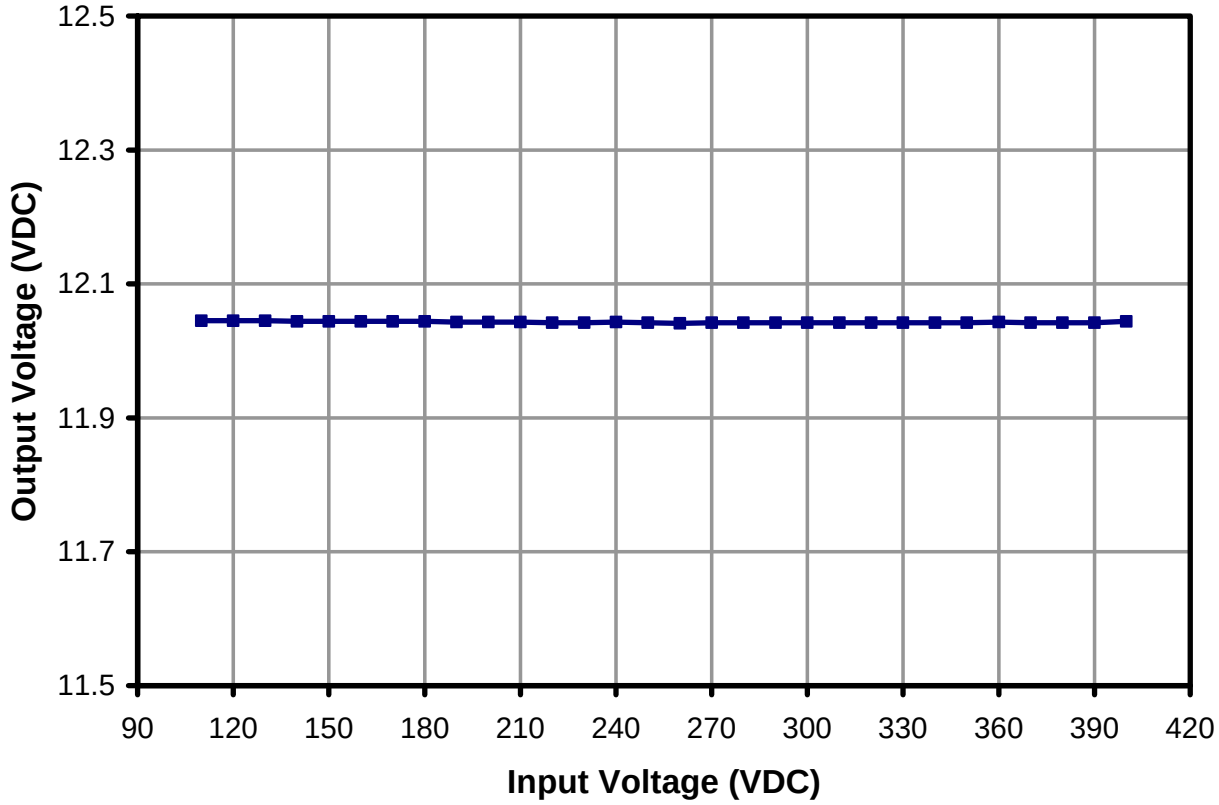

Figure 12 – Line Regulation, Room Temperature, Full Load.

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10 Thermal Performance

10.1 Thermal Test Results at Room Temperature

Test result after 2 hours running continuously at full-load at 110 VDC open frame on bench at room temperature.

Item	Temperature (°C)
	110 VDC
Ambient	25
Transformer (T1)	53.2
TOP265KG (U1)	76.7
Snubber Diode (D1)	54.5
Snubber TVS (VR1)	46.5
Output Diode (D4)	79.5
Output Capacitor (C9)	55
Secondary Snubber Resistor (R14)	57.2
Secondary Snubber Capacitor (C8)	57.5

Table 4 – Room Temperature Data.

10.2 Thermal Scan at Room Temperature

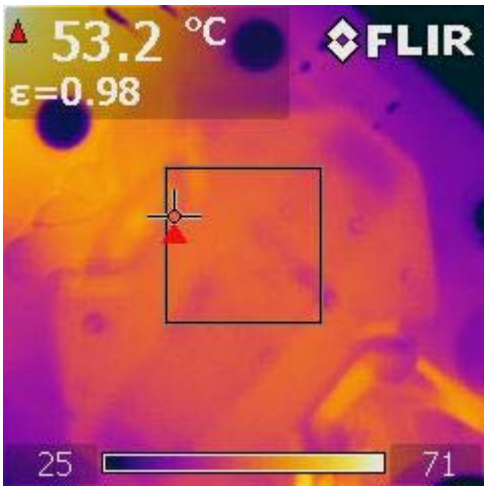

Figure 13 – Transformer Thermal Scan.

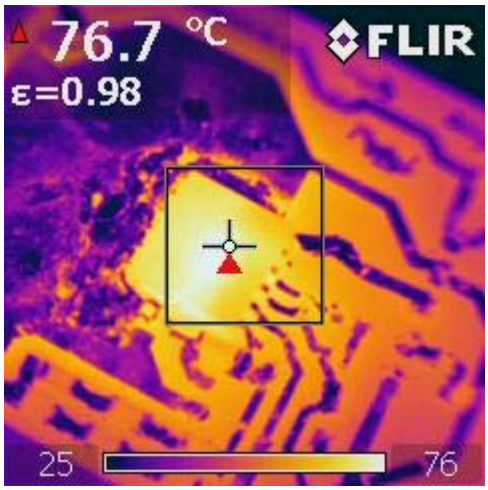

Figure 14 – TOP265KG Thermal Scan.

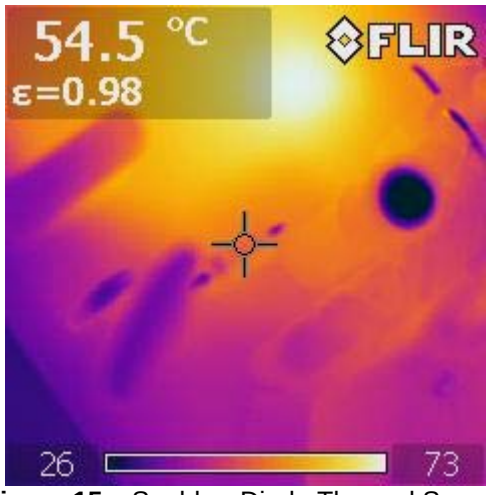

Figure 15 – Snubber Diode Thermal Scan.

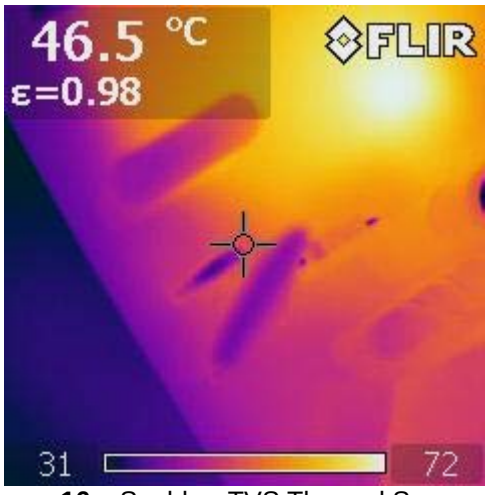

Figure 16 – Snubber TVS Thermal Scan.

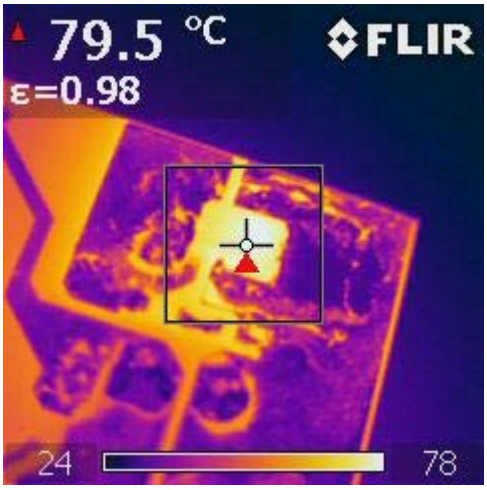

Figure 17 – Output Diode Thermal Scan.

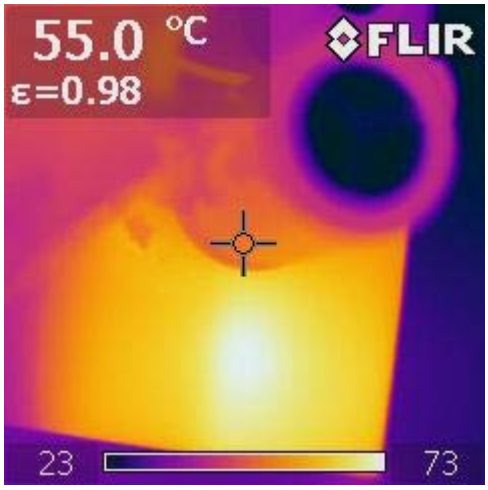

Figure 18 – Output Capacitor Thermal Scan.

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10.3 Thermal Chamber Test Data

Test result after 2 hours running continuously at full-load by using thermal chamber. All measurements made using thermocouples attached to individual components on the circuit board

Item	Temperature (°C)	
	110 VDC	400 VDC
Ambient	40.6	41
Transformer (T1)	67.5	70.9
TOP265KG (U1)	86.1	88.7
Snubber Diode (D1)	71.2	70.4
Snubber TVS (VR1)	66.8	65.9
Output Diode (D4)	102.5	102.8
Output Capacitor (C9)	67	63.5

Table 5 – Thermal Chamber Temperature Data at 40°C.

Item	Temperature (°C)	
	110 VDC	400 VDC
Ambient	50.4	50.5
Transformer (T1)	76.8	78.3
TOP265KG (U1)	96.4	98.4
Snubber Diode (D1)	80.2	78.9
Snubber TVS (VR1)	76.2	73.9
Output Diode (D4)	111.5	112
Output Capacitor (C9)	75	72.5

Table 6 – Thermal Chamber Temperature Data at 50°C.

11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

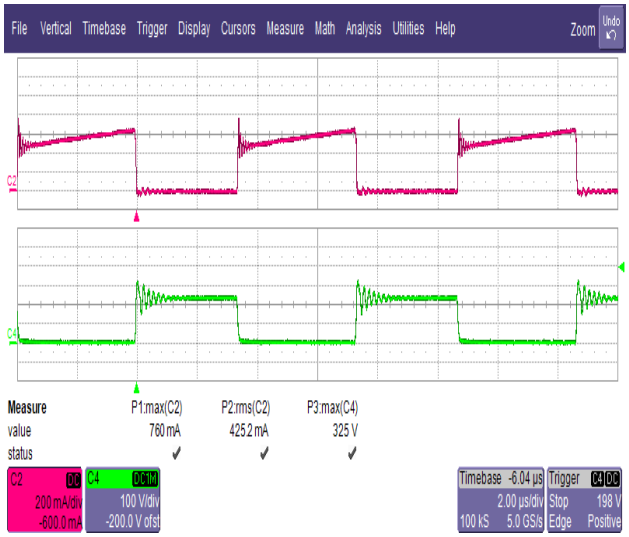

Figure 19 – 110 VDC, Full Load.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V, 2 µs / div.

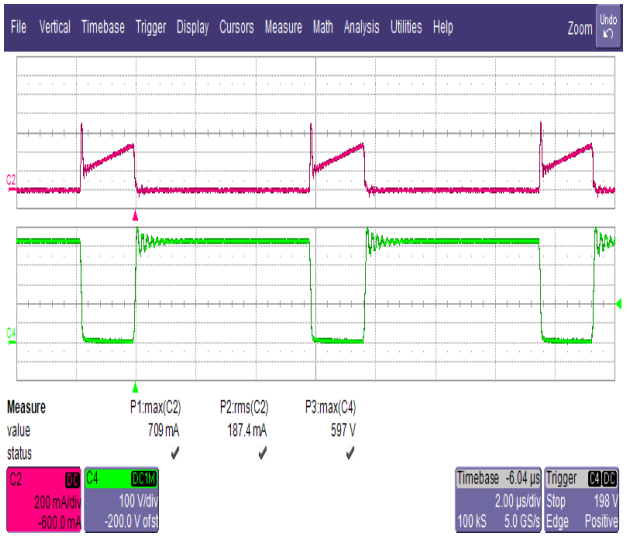

Figure 20 – 400 VDC, Full Load.
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V, 2 µs / div.

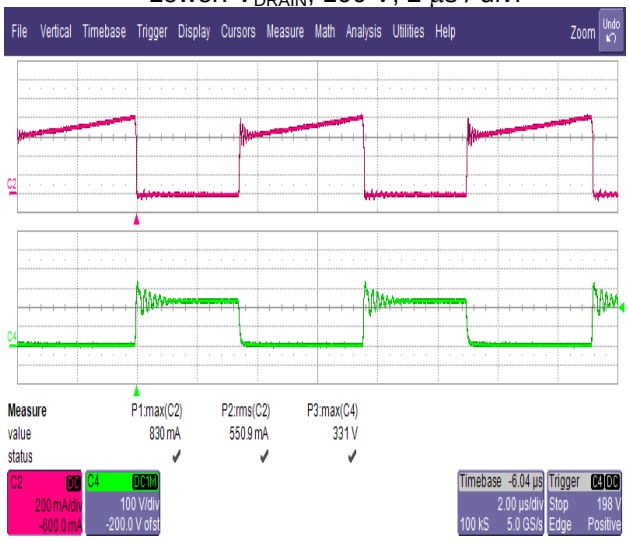

Figure 21 – 110 VDC, Over Load (125%).
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V, 2 µs / div.

Figure 22 – 400 VDC, Over Load (125%).
Upper: I_{DRAIN}, 0.2 A / div.
Lower: V_{DRAIN}, 100 V, 2 µs / div.

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11.2 Rectifier Peak Inverse Voltage (PIV)

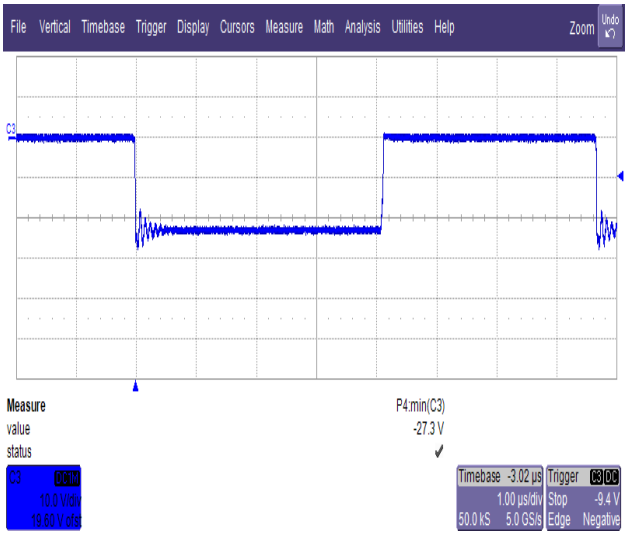

Figure 23 – 110 VDC 100% Load.
10 V / div., 1 µs / div.

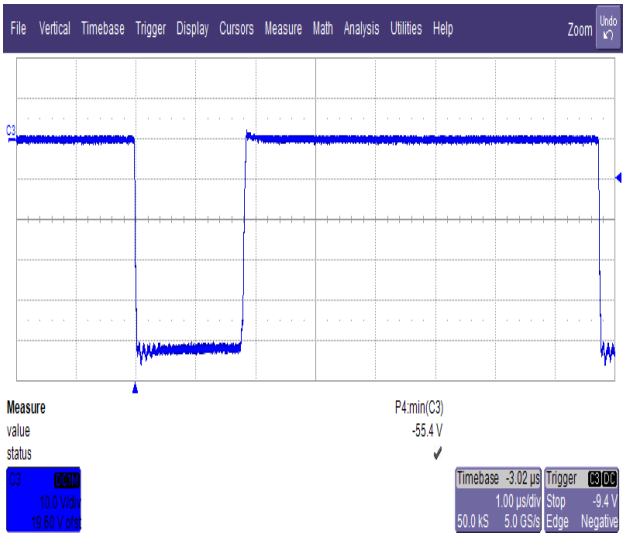

Figure 24 – 400 VDC 100% Load.
10 V / div., 1 µs / div.

11.3 Output OVP Profile

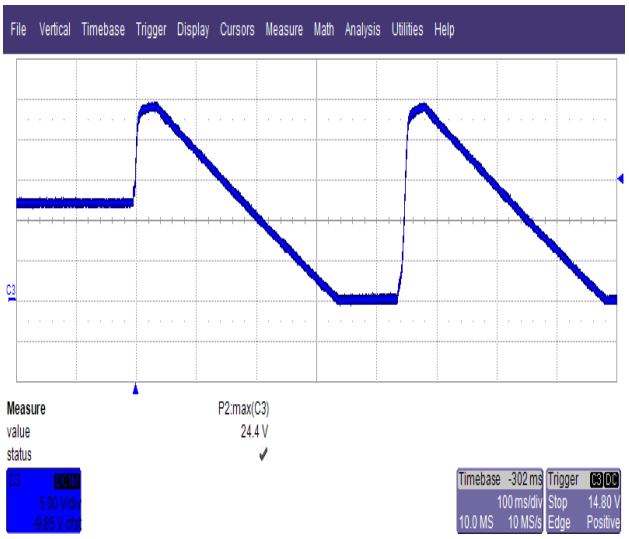

Figure 25 – OVP Profile, 110 VDC, 100 mA Load.
5 V / div. & 100 ms / div.

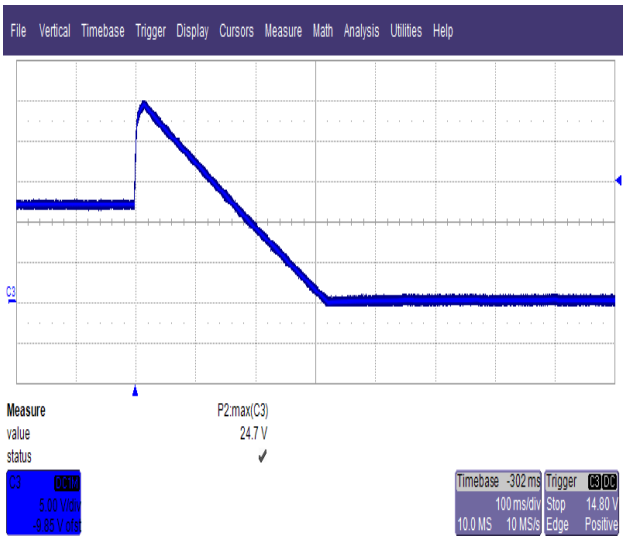

Figure 26 – OVP Profile, 380 VDC, 100 mA Load.
5 V / div. & 100 ms / div.

11.4 OCP Profile

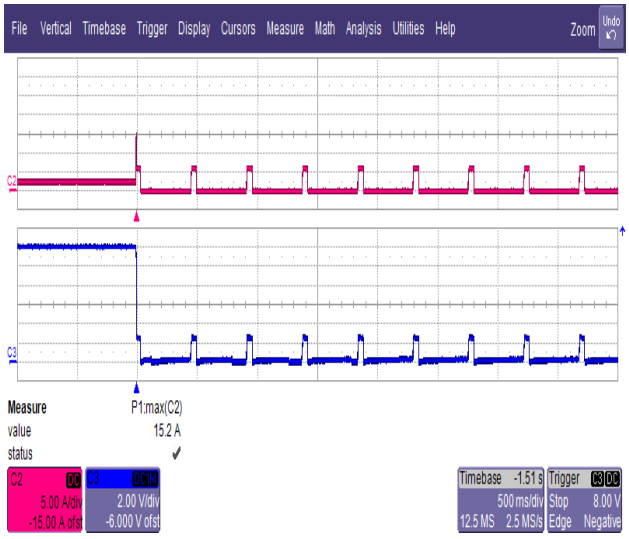

Figure 27 – OCP Profile, 110 VDC.
Upper: I_{OUT}, 5 A / div.
Lower: V_{OUT}, 2 V, 500 ms / div.

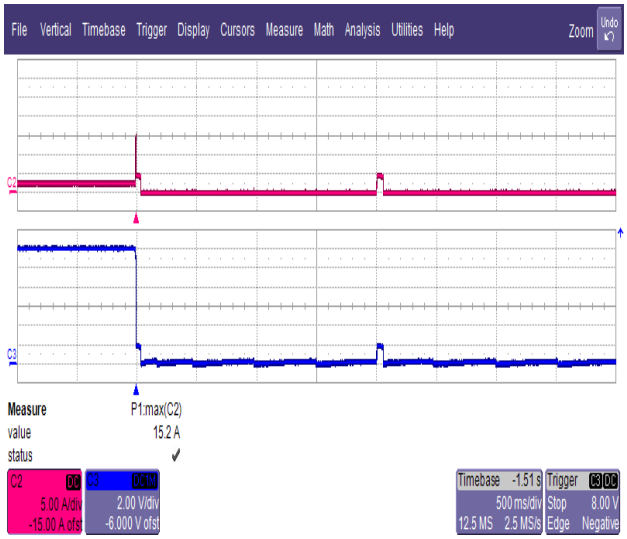

Figure 28 – OCP Profile, 400 VDC.
Upper: I_{OUT}, 5 A / div.
Lower: V_{OUT}, 2 V, 500 ms / div.

11.5 Load Transient Response (50% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.

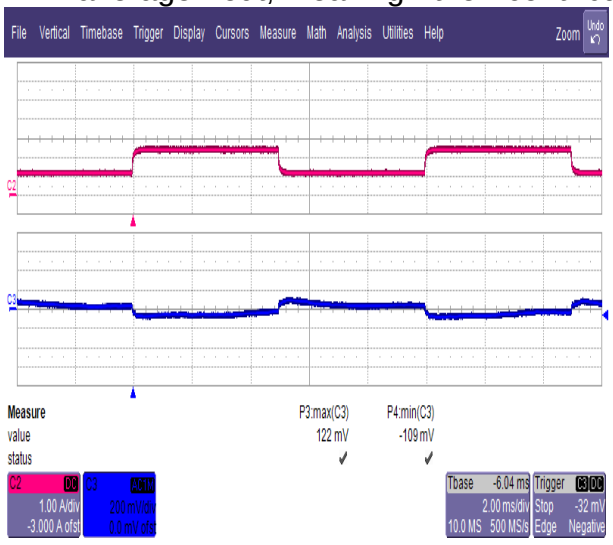

Figure 29 – Transient Response, 110 VDC.
50-100-50% Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: $V_{OUT,}$ 0.2 V / div., 2 ms / div.

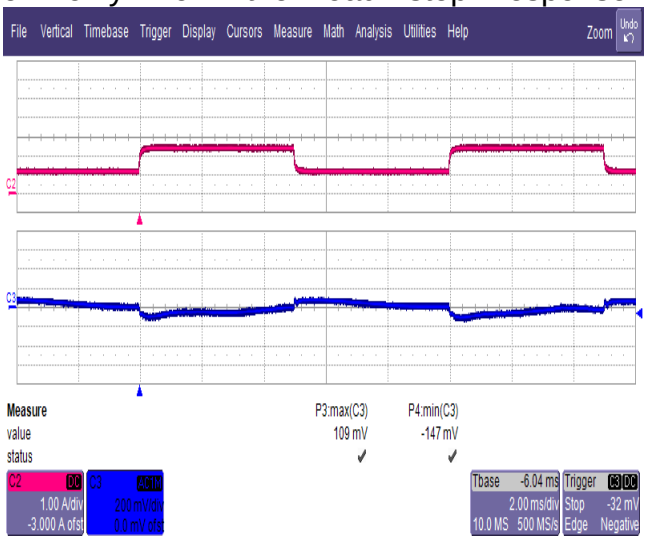

Figure 30 – Transient Response, 380 VDC.
50-100-50% Load Step.
Upper: I_{LOAD}, 1 A / div.
Lower: V_{OUT}, 0.2 V / div., 2 ms / div.

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11.6 Output Ripple Measurements

11.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

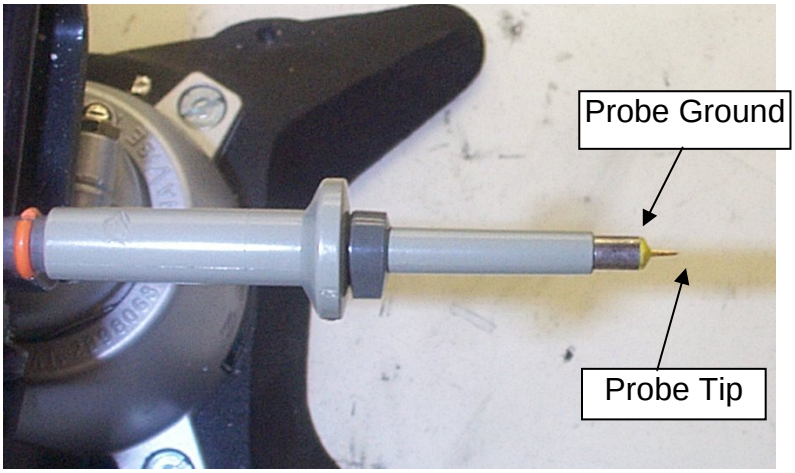

Figure 31 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

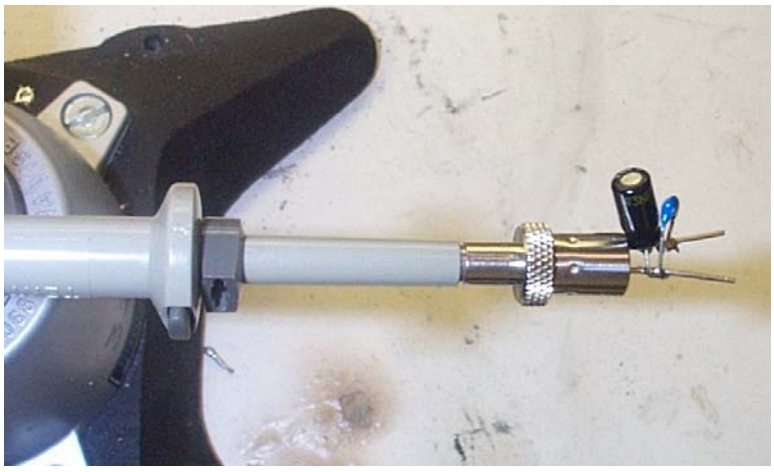

Figure 32 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter.
(Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

11.6.2 Measurement Results

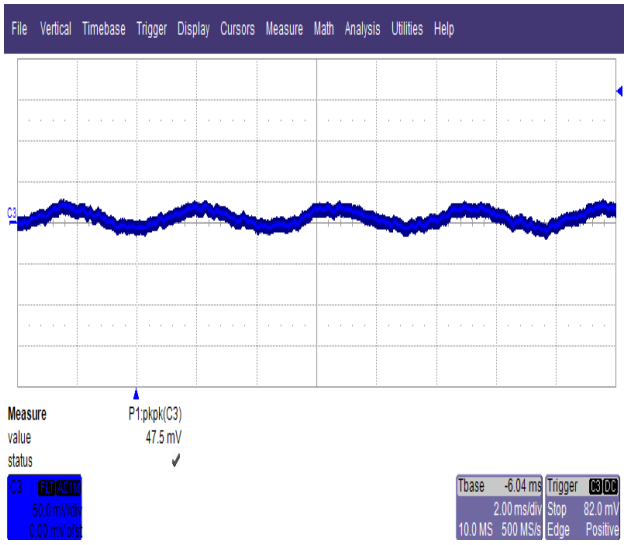

Figure 33 – Output Voltage Ripple, 110 VDC, Full Load. 2 ms, 50 mV / div.

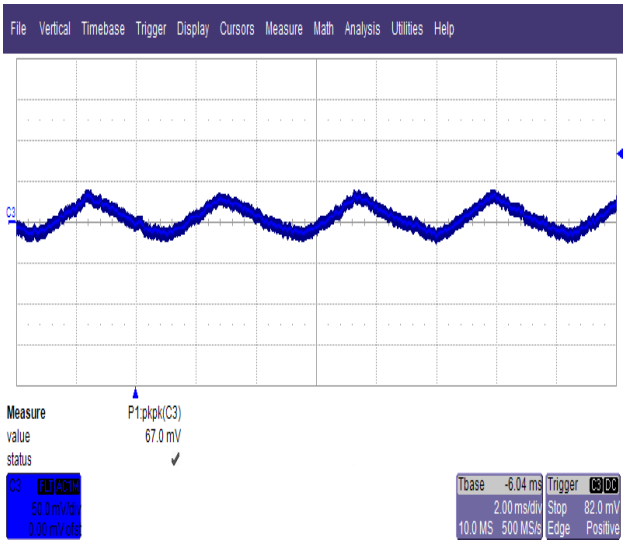

Figure 34 – Output Voltage Ripple, 380 VDC, Full Load. 2 ms, 50 mV / div.

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12 Control Loop Measurements

EQUIPMENT: Frequency Response Analyzer
Model 5060A
VENABLE

12.1 110 VDC Maximum Load

Figure 35 – Gain-Phase Plot, Maximum Steady-State Load.
Vertical Scale: Gain = 10 dB / div., Phase = 30 ° / div.
110 VDC – Crossover Frequency = 2.3 kHz Phase Margin = 50°.

12.2 380 VDC Maximum Load

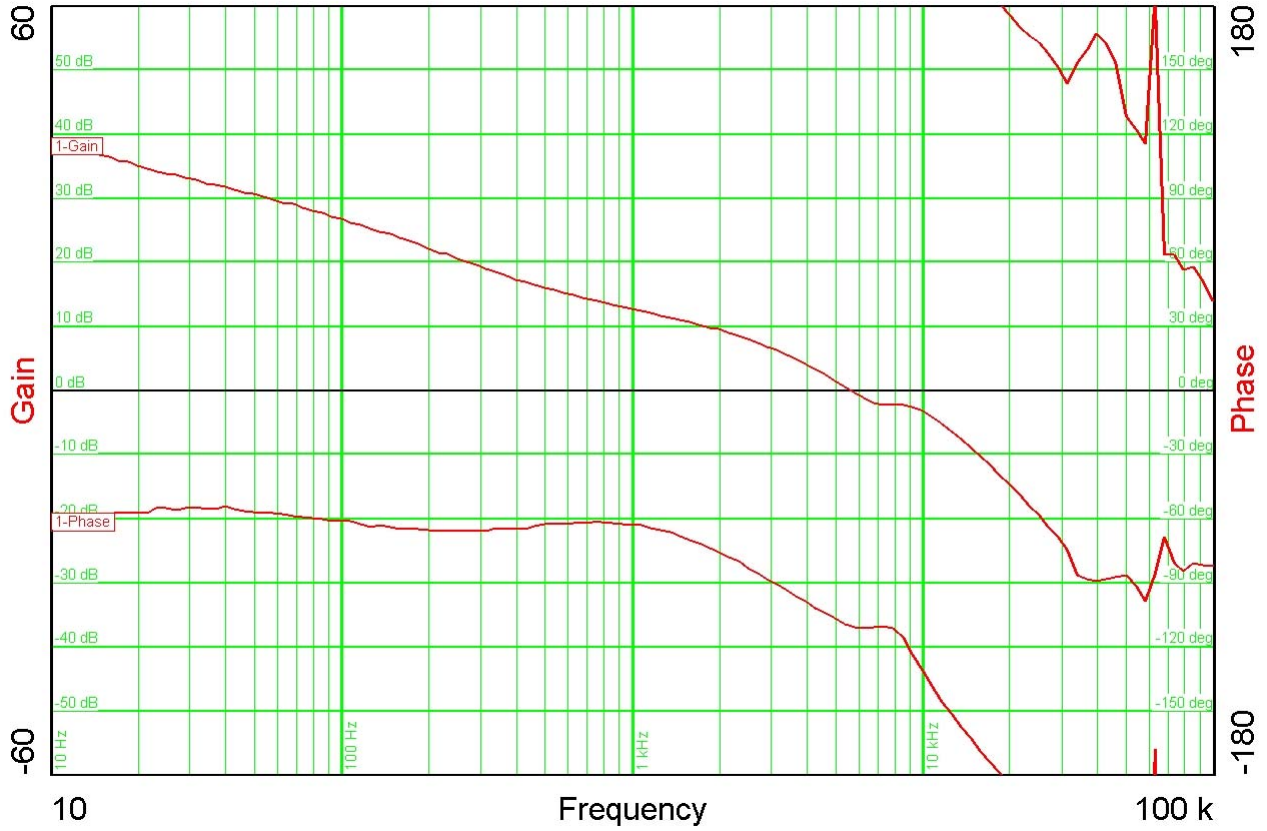

Figure 36 – Gain-Phase Plot, Maximum Steady-State Load.
Vertical Scale: Gain = 10 dB / div., Phase = 30 ° / div.
380 VDC - Crossover Frequency = 5.5 kHz Phase Margin = 70°.

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13 Revision History

Date	Author	Revision	Description & changes	Reviewed
07-Apr-11	SS	1.5	Initial Release	Apps & Mktg

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